REMARKS

Applicant thanks the examiner for the courtesy shown to their attorneys in a telephone interview on July 29, 2005. During the interview the examiner suggested that the applicant amend the claims to replace the recitation "such that no two memory blocks are refreshed at the same time," with language that would more clearly and definitely distinguish the claims from the prior art. The examiner indicated that she would consider the amendment under 37 CFR 1.116

I. Status of Claims

Claims 1-21 are pending.

Claims 1-21 stand rejected.

Claims 1, 8 and 16 are amended herein

II. Claim Rejections Under 35 U.S.C. § 102(b)

The examiner rejected claims 1-21 as being anticipated by Leung, Pub. No. US 2001/0007538 A1.

Independent Claims 1, 8 and 16. As amended, independent claims 1, 8 and 16 each recite "preventing more than one memory block from being refreshed at the same time." Leung discloses a memory device wherein "daisy-chained connections sequentially pass the refresh request signal to the memory banks" Page 2, paragraph [0013] and Fig. 1 at 1000-1127. Leung often refreshes one memory block at a time. But

the memory refresh system disclosed by Leung does not prevent more than one memory block from being refreshed at the same time, and Leung's system does allow two memory blocks to be refreshed at the same time.

In Leung, the actual refresh of a memory block can be delayed until the next clock cycle if that memory block is being read from. As Leung discloses: "When the refresh request signal is activated, a memory bank executes a refresh cycle if there is no access conflict. Otherwise, the refresh cycle is delayed until there is no access conflict." Page 2 paragraph [0013] (emphasis added). The delay can be anywhere from 0 clock cycles up to 256 clock cycles. Page 11 paragraph [0143].

With reference to Figure 1, if a refresh signal to block 1000 is made at clock cycle 1 and there is a delay of one clock cycle in the refresh of block 1000 because of a read operation to block 1000 during clock cycle 1, block 1000 will be refreshed during clock cycle 2. But the daisy chain of the refresh signal from block 1000 to block 1001 would not be delayed by the read operation, and therefore the signal to refresh block 1001 would also take place during clock cycle 2. This is because the daisy chain flip-flops 321 (Fig. 3) are tied to the clock signal and the refresh inputs to one block REQI[n] are shifted out to the next block REQI[n+1] via signal REQO[n] during each clock cycle. See Fig. 3, which shows that REQI[n] is clocked out to REQO[n] by D flip flop 321, and page 5, paragraph [0060] which states "the input refresh request signal REQI[n] is latched into D-register 321 in response to the rising edge of the Clk signal.

But the internal refresh signal for memory block "n" can be delayed depending on the status of memory access signals BA[n], Mrd and Mwr. Fig. 3. Thus in Leung a single cycle read to any memory block at the same time as a pending refresh signal to that block will nearly always result in more than one memory block being refreshed at the same time, when that delayed refresh takes place at the same time that the subsequent block is being refreshed.

By the claim amendment and the above remarks, the applicant asserts that the examiner's rejection of Claims 1, 8 and 16 cannot be sustained, and requests that Claims 1, 8 and 16 be allowed as presently amended for at least the remarks stated above.

Claims 2 - 7. By the claim amendment to independent Claim 1 and the remarks regarding Claim 1 herein, the applicant asserts that the examiner's rejection of Claim 1 cannot be sustained, and requests that Claims 2 through 7, which depend from Claim 1 be allowed.

Claim 8. Claim 8 requires that "all memory blocks have a refresh controller contained therein." The examiner has rejected Claim 8, citing Leung as teaching that "all memory blocks have a refresh controller contained therein which would enable sequential refresh of the subsequent memory blocks (page 2 paragraph [0014] and [0011])." Contrary to the examiner's assertion, the reference citation makes clear that there is only one refresh controller in the system disclosed in Leung, not that all memory blocks have a refresh controller contained therein. "The memory controller ensures that each memory bank, the read buffer and the write buffer, are properly

refreshed during the proper refresh period." Page 2 paragraph [0014]. I.e. one controller, in the singular form controls each memory bank. Figure 1 confirms this, there is only one memory controller 108, one refresh address counter 101 and one refresh timer 102 in the system.

By the claim amendment and the remarks herein, the applicant asserts that the examiner's rejection of Claim 8 cannot be sustained, and requests that Claim 8 be allowed as presently amended.

Claims 9, 10, 12 - 15. By the claim amendment to independent Claim 8 and the remarks regarding Claim 8 herein, the applicant asserts that the examiner's rejection of Claim 8 cannot be sustained, and requests that Claims 9, 10, 12 -15, which depend from Claim 8, be allowed.

Claim 11 and 18. With respect to Claim 11, the examiner has cited Leung as disclosing "wherein the refresh controller of each memory block generates a refresh request [RFREQ] for an immediately subsequent memory block when the memory block it belongs to is being refreshed. (Page 4, paragraph [0047])." With respect to Claim 18, the examiner has cited the same paragraph in Leung as disclosing "wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to and a refresh request [RFREQ] for an immediately subsequent memory block when the memory block it belongs to is being refreshed."

Leung does not disclose nor suggest that the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed. Leung discloses a daisy-chained series of "D" registers, (321, Fig. 3) one in each memory block, that sequentially clock refresh requests to each next memory block on every clock cycle. Page 4, paragraph [0047]. "The refresh request to the memory blocks is thus generated by a daisy chain formed by the D registers connecting to the REQI and REQO terminals of the memory blocks 1000-1127."

Leung does not disclose that the sequential refresh request to the next sequential block occurs while a first block is being refreshed. To the contrary, as explained in detail above, the refresh of any particular block can be delayed if there is a memory request to that block, yet the D register in the block will still cause the refresh out signal (REQO) to propagate to the next sequential block. Thus the refresh request for a subsequent memory block will be generated even if the previous memory block is not being refreshed but rather the refresh of the previous memory block is delayed because of a memory access.

Because of the remarks herein regarding Claim 11 and 18 and the amendment and remarks to independent Claims 8 and 16 from which Claims 11 and 18 depend respectively, the applicant asserts that the examiner's rejection of Claims 11 and 18

cannot be sustained and requests that Claims 11 and 18 be allowed.

Claim 16. Claim 16 requires that "all memory blocks have a refresh controller contained therein." The examiner has rejected Claim 16, citing Leung as teaching that "all memory blocks have a refresh controller contained therein which would enable sequential refresh of the subsequent memory blocks (page 2 paragraph [0014] and [0011])." As stated above, contrary to the examiner's assertion, there is only one refresh controller in the system disclosed in Leung, all memory blocks do not have a refresh controller contained therein. Figure 1 confirms this, there is only one memory controller 108, one refresh address counter 101 and one refresh timer 102.

By the claim amendment and the remarks herein, the applicant asserts that the examiner's rejection of Claim 16 cannot be sustained and requests that Claim 16 be allowed as presently amended.

Claims 17, 19 - 21. By the claim amendment to independent Claim 16 and the remarks regarding Claim 16 herein, the applicant asserts that the examiner's rejection of Claim 16 cannot be sustained, and requests that Claims 17, 19 - 21, which depend from Claim 16, be allowed.

III. Conclusion

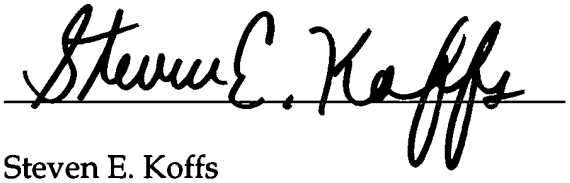
Having addressed the examiner's rejections, applicant submits that the reasons for the examiner's rejections have been overcome by the amendments and remarks made herein, and the rejections can no longer be sustained. Applicant respectfully

requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued.

Should any unresolved issues remain, the examiner is requested to call Applicant's attorney at the telephone number below.

The Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may be associated with this communication to Duane Morris LLP deposit account 04-1679.

Respectfully submitted,



Steven E. Koffs
Registration No. 37,163,
Attorney For Applicant

DUANE, MORRIS LLP
One Liberty Place
Philadelphia, Pennsylvania 19103-7396
215-979-1250 (Telephone)
215-979-1020 (Fax)

PHI\1478834.1